## AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

**Listing of Claims:**

1. (currently amended) An apparatus comprising:

a converter circuit coupled to receive a plurality of dynamic logic input signals, in which the converter circuit has a plurality of input transistors gated by the plurality of dynamic logic input signals, including a first pair of complementary metal-oxide-semiconductor (CMOS) transistors coupled to be gated by a first of the dynamic logic input signals, to generate a logical combination of the plurality of dynamic logic input signals as a static logic output signal on an output node ~~responsive to the dynamic logic input signal~~ during an evaluate phase of a clock signal, the static logic output signal having a first state or a second state depending on the dynamic logic input signals, the converter circuit further including a first clocked transistor to be active to enable the first pair of CMOS transistors during the evaluate phase, but to float the output node to retain the state of the static logic output signal during a precharge phase of the clock signal when a precharge voltage is to be applied to gate inputs of the first pair of CMOS transistors; and

a noise suppression circuit, including a second pair of CMOS transistors coupled to be gated by a feedback voltage from the output node, to sustain the state of the output node during the precharge phase, the noise suppression circuit further including a second clocked transistor which is to be ~~enabled~~ active during the precharge phase to couple a first potential onto the output node through the second clocked transistor and one of the second pair of CMOS transistors when the output node is in the first state, but to couple a second potential through the other of the second pair of CMOS transistors and one of the first pair of CMOS transistors of the converter circuit when the output node is in the second state.

2. (canceled)

3. (canceled)

4. (currently amended) The apparatus as recited in claim ~~2~~ 1 wherein the first clocked transistor is a NMOS transistor and the second clocked transistor is a PMOS transistor.

5. (currently amended) The apparatus as recited in claim ~~2~~ 1 wherein the first potential placed on the output node is coupled from a supply voltage and the second potential placed on the output node is coupled from ground.

6. (previously presented) The apparatus as recited in claim 5 wherein the converter circuit operates as an inverter.

7. (previously presented) The apparatus as recited in claim 6 wherein the feedback voltage is an inverted state of the static logic output signal.

8-9. (canceled)

10. (previously presented) The apparatus as recited in claim 1 wherein the transistors of the noise suppression circuit are sized between approximately 30%-50% of the transistors in the converter circuit.

11. (previously presented) The apparatus as recited in claim 1 wherein the transistors of the noise suppression circuit are sized approximately 30% of the transistors in the converter circuit.

12. (previously presented) The apparatus as recited in claim 1 wherein the transistors of the converter circuit and the noise suppression circuit are sized according to an expected noise on the output node.

13. (currently amended) A circuit comprising:

a converter circuit coupled to receive a plurality of dynamic logic input signals, in

which the converter circuit has a plurality of input transistors gated by the plurality of dynamic logic input signals, the converter circuit having a first pair of complementary metal-oxide-semiconductor (CMOS) transistors and a first clocked transistor coupled in series between a supply voltage node and a supply return node and in which an output node is obtained at a junction of the first pair of CMOS transistors, the first pair of CMOS transistors coupled to be gated by a first of the dynamic logic input signals to generate a logical combination of the plurality of dynamic logic input signals as a static logic output signal onto the output node during an evaluate phase of a clock signal when the clock signal activates the first clocked transistor to enable the converter circuit, but during a precharge phase of the clock signal when a precharge voltage is to be applied to gate inputs of the first pair of CMOS transistors, the first clocked transistor is deactivated to float the output node to retain existing state of the static logic output signal; and

a noise suppression circuit having a second pair of CMOS transistors and a second clocked transistor, in which one of the second pair of CMOS transistors and the second clocked transistor are coupled in series between the supply voltage node and the output node and other of the second pair of CMOS transistors and one of the transistors of the first pair of CMOS transistors of the converter circuit are coupled in series between the output node and the supply return node, the second pair of CMOS transistors gated by a feedback voltage from the output node to either place a supply voltage potential from the supply voltage node or supply return potential from the supply return node onto the output node during the precharge phase to maintain the state of the static logic output signal to suppress noise on the output node.

14. (previously presented) The circuit as recited in claim 13 wherein the first clocked transistor is a NMOS transistor and the second clocked transistor is a PMOS transistor.

15. (previously presented) The circuit as recited in claim 14 wherein the one of the second pair of CMOS transistors and the second clocked transistor coupled between the supply voltage node and the output node are PMOS transistors and wherein the other of the second pair of CMOS transistors and one of the transistors of the first pair of CMOS transistors coupled between the output node and the supply return node are NMOS

transistors.

16. (canceled)

17. (previously presented) The circuit as recited in claim 15 wherein the transistors of the noise suppression circuit are sized between approximately 30%-50% of the transistors in the converter circuit.

18. (previously presented) The circuit as recited in claim 15 wherein the transistors of the noise suppression circuit are sized approximately 30% of the transistors in the converter circuit.

19-21. (canceled)